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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/814,868	03/30/2004	Christopher J. Diorio	IMPJ-0027C	5625

49684 7590 05/03/2006

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EXAMINER	
MAI, SON LUU	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 05/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/814,868	DIORIO ET AL.	
	Examiner	Art Unit	
	Son L. Mai	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-73* is/are pending in the application.

4a) Of the above claim(s) *16-64 and 66-70* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-12,65 and 71-73* is/are rejected.

7)☒ Claim(s) *4 and 13-15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3-30-04;8-2-04;2-10-05;12-15-05;1-23-06;2-27-06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of Group I (claims 1-15, 65 and 71-73) in the reply filed on 09-16-05 is acknowledged. The traversal is on the ground(s) that "Each alleged species of claims appears to be clearly related to each other. No separate art classifications have been provided." This is not found persuasive because the species direct to distinct reprogrammable fuse apparatuses. And the search for one species does not encompass others. The requirement is still deemed proper and is therefore made FINAL.

2. Claims 16-64 and 66-70 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to nonelected species, there are no allowable generic or linking claim.

Specification

3. The disclosure is objected to because of the following informalities:

On page 1, the information of related cases are missing.

In paragraph [0045], line 4, "a" before "an" should be deleted.

In paragraph [0054], line 10, the Serial Number is incomplete. Appropriate correction is required.

4. Claims 2-15 are objected to because of the following informalities:

In claims 2-15, the "electronic fuse array" should be changed to "reprogrammable fuse apparatus" for lacking of antecedent basis.

Claim 8 is incomplete as written.

In Claim 71, in line 3, "a logic set and reset input" should read –logic set and reset inputs— and in line 5, "said output state" lacks antecedent basis in the claim.

In claim 73, in line 3-4, the specification does not provide support for the magnitude of a signal on the set and reset inputs. Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-3, 5-12 and 65 are rejected under 35 U.S.C. 102(e) as being anticipated by Madurawe (U.S. Patent Application Publication US 20050149896 A1)

Regarding claims 1 and 65, Madurawe teaches a reprogrammable fuse apparatus, comprising: a plurality of rewriteable electronic fuses (figure 2D), each having a nonvolatile memory element, arrayed in a predetermined configuration; and a plurality of high-voltage switches (350 in figure 3B), each high-voltage switch corresponding to an associated electronic fuse of said plurality of electronic fuses, and each high-voltage switch having a high-voltage input terminal (Vcc) and a fuse-state state-setting input terminal (Din), wherein a given electronic fuse of the plurality of electronic fuses is programmed by selecting and coupling an associated control signal to the given electronic fuse.

Regarding claim 2, Madurawe teaches each electronic fuse comprises a CMOS latch having two cross-coupled inverters (303 and 304 in figure 3A).

Regarding claim 3, Madurawe discloses the nonvolatile memory element of each electronic fuse comprises a floating-gate transistor (240 in figure 2D) having a floating gate, an amount of charge on the floating gate of any given nonvolatile memory element determining a memory value of the given nonvolatile memory element.

Regarding claim 5, Madurawe teaches the nonvolatile memory elements are manufactured in a standard CMOS fabrication process (see paragraph [0020]).

Regarding claim 6, Madurawe teaches each floating-gate transistor of each electronic fuse is a transistor selected from the group consisting of: nFET, pFET, FinFET, and multi-gate FET (figure 2D shows an nFET floating gate transistor).

Regarding claim 7, Madurawe teaches the nonvolatile memory element of each electronic fuse is a memory element using a mechanism selected from the group consisting of magnetoresistive, ferroelectric, phase-change, and dielectric, for nonvolatile storage of information (see paragraph [0017]).

Regarding claims 8-12, Madurawe describes at paragraph [0010] the inherent features of a floating-gate transistor as claimed.

7. Claims 71-73 are rejected under 35 U.S.C. 102(e) as being anticipated by Smith et al. (U.S. Patent 6,693,819).

Regarding claim 71, Smith teaches a programmable fuse element (fuses 25 and 27 in figure 2) for providing one of two fuse states (low or high states), comprising: a

logic set and reset inputs (progp and progpb signals in figure 3); voltage inputs for ground (0 V), Vdd (VDD25 in figure 3), intermediate-voltage (readvdd) and high-voltage (VPP); and at least one output (hv_bit) indicating an output state.

Regarding claim 72, Smith's apparatus further comprises an initialize input (lv_bit signal is set low or high) for initializing the fuse element.

Regarding claim 73, Smith teaches that a magnitude of a signal on the at least one output (hv_bit is set at high or 5 volts; see column 8, lines 1-12) is as large as a magnitude of the high-voltage voltage input (VPP = 5 volts) and a magnitude of a signal on the set and reset inputs (progp and progpb are set at 2.5 volts) is less than the magnitude of the high-voltage voltage input (VPP = 5 volts).

Allowable Subject Matter

8. Claims 4, 13-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record fails to teach the further limitation of claims 1, 3 and 4 in combination, in which each nonvolatile memory element includes a first capacitor. Each first capacitor of any given nonvolatile memory element having a first plate in common with the floating gate of the floating-gate transistor of the given nonvolatile memory element.

Conclusion

10. The prior art made of record cited on Form PTO-892 is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Son L. Mai whose telephone number is 571-272-1786. The examiner can normally be reached on 8am to 6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

04-27-06

Son L. Mai
Primary Examiner
Art Unit 2827